THAT WHICH IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate; and

at least one MOSFET adjacent said substrate and comprising

a superlattice channel including a plurality of stacked groups of layers, and

source and drain regions laterally adjacent said superlattice channel and a gate overlying said superlattice channel for causing transport of charge carriers through said superlattice channel in a parallel direction relative to the stacked groups of layers,

each group of layers of said superlattice channel comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

said energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that said superlattice channel has a higher charge carrier mobility in the parallel direction than would otherwise be present.

2. A semiconductor device according to Claim 1 wherein said superlattice channel has a common energy band structure therein.

3. A semiconductor device according to Claim 1 wherein the charge carriers having the higher mobility comprise at least one of electrons and holes.

4. A semiconductor device according to Claim 1 wherein each base semiconductor portion comprises silicon.

5. A semiconductor device according to Claim 1 wherein each energy band-modifying layer comprises oxygen.

6. A semiconductor device according to Claim 1 wherein each energy band-modifying layer is a single monolayer thick.

7. A semiconductor device according to Claim 1 wherein each base semiconductor portion is less than eight monolayers thick.

8. A semiconductor device according to Claim 1 wherein each base semiconductor portion is two to six monolayers thick.

9. A semiconductor device according to Claim 1 wherein said superlattice further has a substantially direct energy bandgap.

10. A semiconductor device according to Claim 1 wherein said superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

11. A semiconductor device according to Claim 11 wherein said gate comprises a gate electrode layer and a gate dielectric layer between said gate electrode layer and said base semiconductor cap layer.

12. A semiconductor device according to Claim 1 wherein all of said base semiconductor portions are a same number of monolayers thick.

13. A semiconductor device according to Claim 1 wherein at least some of said base semiconductor portions are a different number of monolayers thick.

14. A semiconductor device according to Claim 1 wherein all of said base semiconductor portions are a different number of monolayers thick.

15. A semiconductor device according to Claim 1 wherein each non-semiconductor monolayer is thermally stable through deposition of a next layer.

16. A semiconductor device according to Claim 1 wherein each base semiconductor portion comprises a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors.

17. A semiconductor device according to Claim 1 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

18. A semiconductor device according to Claim 1 wherein the higher mobility results from a lower conductivity effective mass for the charge carriers in the parallel direction than would otherwise occur.

19. A semiconductor device according to Claim 18 wherein the lower conductivity effective mass is less than two-thirds the conductivity effective mass that would otherwise occur.

20. A semiconductor device according to Claim 1 wherein said superlattice further comprises at least one type of conductivity dopant therein.

21. A semiconductor device comprising:

a substrate; and

at least one MOSFET adjacent said substrate and comprising

a superlattice channel comprising a plurality of stacked groups of layers, and

source and drain regions laterally adjacent said superlattice channel and a gate overlying said superlattice channel for causing transport of charge carriers through said superlattice channel in a parallel direction relative to the stacked groups of layers,

each group of layers of said superlattice channel comprising a plurality of stacked silicon atomic layers defining a silicon portion and an energy band-modifying layer thereon,

said energy-band modifying layer comprising at least one oxygen atomic layer

constrained within a crystal lattice of adjacent silicon portions so that said superlattice has a higher charge carrier mobility than would otherwise be present.

22. A semiconductor device according to Claim 21 wherein said superlattice channel has a common energy band structure therein.

23. A semiconductor device according to Claim 21 wherein the charge carriers having the lower conductivity effective mass comprise at least one of electrons and holes.

24. A semiconductor device according to Claim 21 wherein each energy band-modifying layer is a single atomic layer thick.

25. A semiconductor device according to Claim 21 wherein each silicon portion is less than eight atomic layers thick.

26. A semiconductor device according to Claim 21 wherein each silicon portion is two to six atomic layers thick.

27. A semiconductor device according to Claim 21 wherein said superlattice channel further has a substantially direct energy bandgap.

28. A semiconductor device according to Claim 21 wherein said superlattice channel further comprises a silicon cap layer on an uppermost group of layers.

29. A semiconductor device according to Claim 29 wherein said gate comprises a gate electrode layer and a gate dielectric layer between said gate electrode layer and said base semiconductor cap layer.

30. A semiconductor device according to Claim 21 wherein all of said silicon portions are a same number of atomic layers thick.

31. A semiconductor device according to Claim 21 wherein at least some of said silicon portions are a different number of atomic layers thick.

32. A semiconductor device according to Claim 21 wherein all of said silicon portions are a different number of atomic layers thick.

33. A semiconductor device according to Claim 21 wherein the higher charge carrier mobility results from a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise occur.

34. A semiconductor device according to Claim 21 wherein said superlattice channel further comprises at least one type of conductivity dopant therein.

35. A semiconductor device comprising:

a substrate; and

at least one MOSFET adjacent said substrate and comprising

a superlattice channel comprising a plurality of stacked groups of layers, and

source and drain regions laterally adjacent said superlattice channel and a gate overlying said superlattice channel for causing transport of charge carriers through said superlattice channel in a parallel direction relative to the stacked groups of layers,

each group of layers of said superlattice channel comprising less than eight stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

said energy-band modifying layer comprising a single non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that said superlattice has a high charge carrier mobility in the parallel direction than would otherwise be present.

36. A semiconductor device according to Claim 35 wherein said superlattice channel has a common energy band structure therein.

37. A semiconductor device according to Claim 35 wherein the charge carriers having the higher mobility comprise at least one of electrons and holes.

38. A semiconductor device according to Claim 35 wherein said superlattice channel further has a substantially direct energy bandgap.

39. A semiconductor device according to Claim 35 wherein said superlattice channel further comprises a base semiconductor cap layer on an uppermost group of layers.

40. A semiconductor device according to Claim 40 wherein said gate comprises a gate electrode layer and a gate dielectric layer between said gate electrode layer and said base semiconductor cap layer.

41. A semiconductor device according to Claim 35 wherein all of said base semiconductor portions are a same number of monolayers thick.

42. A semiconductor device according to Claim 35 wherein at least some of said base semiconductor portions are a different number of monolayers thick.

43. A semiconductor device according to Claim 35 wherein all of said base semiconductor portions are a different number of monolayers thick.

44. A semiconductor device according to Claim 35 wherein the higher charge carrier mobility results from a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise occur.

45. A semiconductor device according to Claim 35 wherein said superlattice channel further comprises at least one type of conductivity dopant therein.

46. A semiconductor device comprising:

a substrate; and

at least one MOSFET adjacent said substrate and comprising

a superlattice channel comprising a plurality of stacked groups of layers, and

source and drain regions laterally adjacent said superlattice channel and a gate overlying said superlattice channel for causing transport of charge carriers through said superlattice channel in a parallel direction relative to the stacked groups of layers,

each group of layers of said superlattice channel comprising less than eight stacked silicon atomic layers defining a silicon portion and an energy band-modifying layer thereon,

said energy-band modifying layer comprising a single oxygen atomic layer constrained within a crystal lattice of adjacent silicon portions.

47. A semiconductor device according to Claim 46 wherein said superlattice channel further comprises a base semiconductor cap layer on an uppermost group of layers.

48. A semiconductor device according to Claim 47 wherein said gate comprises a gate electrode layer and

a gate dielectric layer between said gate electrode layer and said base semiconductor cap layer.

49. A semiconductor device according to Claim 46 wherein all of said base semiconductor portions are a same number of atomic layers thick.

50. A semiconductor device according to Claim 46 wherein at least some of said base semiconductor portions are a different number of atomic layers thick.

51. A semiconductor device according to Claim 46 wherein all of said base semiconductor portions are a different number of atomic layers thick.

52. A semiconductor device according to Claim 46 wherein said superlattice channel further comprises at least one type of conductivity dopant therein.

53. A semiconductor device comprising:

a substrate; and

at least one MOSFET adjacent said substrate and comprising

a superlattice channel including a plurality of stacked groups of layers, and

source and drain regions laterally adjacent said superlattice channel and a gate overlying said superlattice channel for causing transport of charge carriers through said superlattice channel in a parallel direction relative to the stacked groups of layers,

each group of layers of said superlattice channel comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

said energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that said superlattice channel has a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise be present.

54. A semiconductor device according to Claim 53 wherein said superlattice channel has a common energy band structure therein.

55. A semiconductor device according to Claim 53 wherein the charge carriers having the lower conductivity effective mass comprise at least one of electrons and holes.

56. A semiconductor device according to Claim 53 wherein each base semiconductor portion comprises silicon.

57. A semiconductor device according to Claim 53 wherein each energy band-modifying layer comprises oxygen.

58. A semiconductor device according to Claim 53 wherein each energy band-modifying layer is a single monolayer thick.

59. A semiconductor device according to Claim 53 wherein each base semiconductor portion is less than eight monolayers thick.

60. A semiconductor device according to Claim 53 wherein each base semiconductor portion is two to six monolayers thick.

61. A semiconductor device according to Claim 53 wherein said superlattice further has a substantially direct energy bandgap.

62. A semiconductor device according to Claim 53 wherein said superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

63. A semiconductor device according to Claim 62 wherein said gate comprises a gate electrode layer and a gate dielectric layer between said gate electrode layer and said base semiconductor cap layer.

64. A semiconductor device according to Claim 53 wherein all of said base semiconductor portions are a same number of monolayers thick.

65. A semiconductor device according to Claim 53 wherein at least some of said base semiconductor portions are a different number of monolayers thick.

66. A semiconductor device according to Claim 53 wherein all of said base semiconductor portions are a different number of monolayers thick.

67. A semiconductor device according to Claim 53 wherein each non-semiconductor monolayer is thermally stable through deposition of a next layer.

68. A semiconductor device according to Claim 53 wherein each base semiconductor portion comprises a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors.

69. A semiconductor device according to Claim 53 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

70. A semiconductor device according to Claim 53 wherein the lower conductivity effective mass is less than two-thirds the conductivity effective mass that would otherwise occur.

71. A semiconductor device according to Claim 53 wherein said superlattice further comprises at least one type of conductivity dopant therein.